Hackathon –2 : IDE + Heater Design

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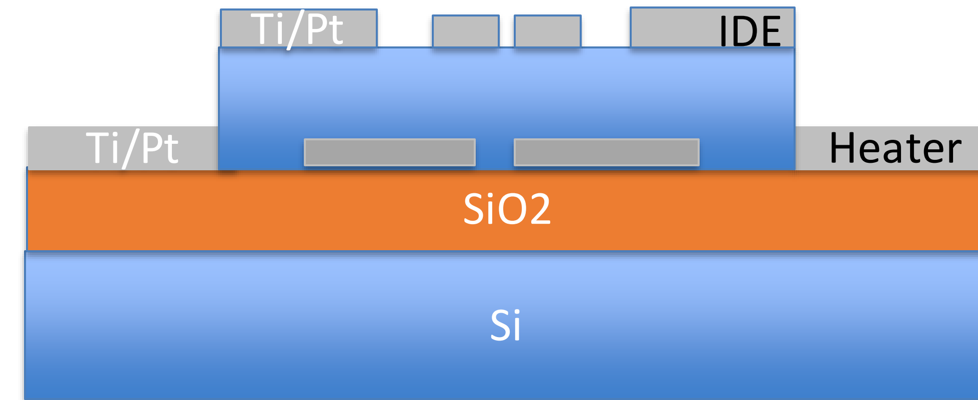
IDE's with micro-heaters

- 4" Si/1um SiO2 wafer + RCA cleaning
- 4 µm PECVD SiO2 deposition as thermal barrier
- Front heater Lithography + 20/100nm Ti/Pt deposition + Liftoff
- 500 nm PECVD SiO2 deposition
- Pad opening Lithography + BOE etch of SiO2 (Landing on Pt)
- IDE Lithography+ 20/100nm- Ti/Pt deposition+ Liftoff

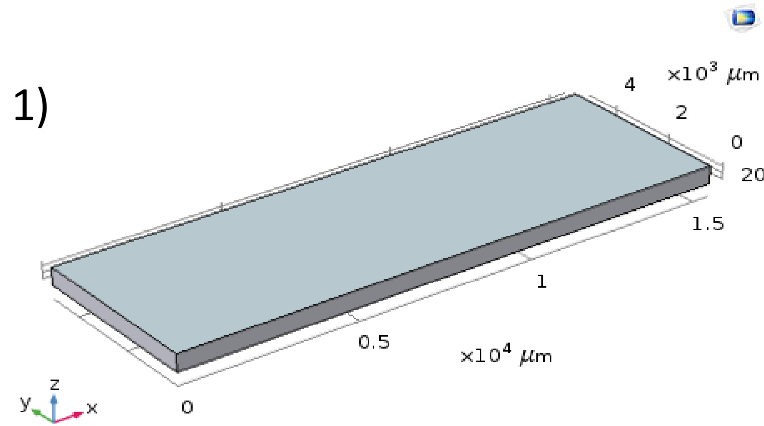


Cross section image

Process Flow

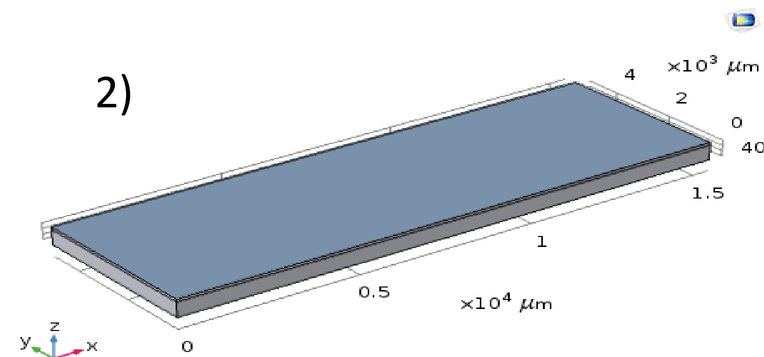
CENSE

1)



Si wafer / RCA Cleaning

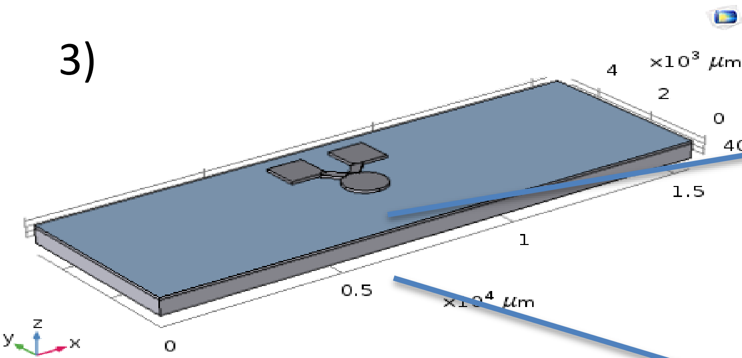
2)

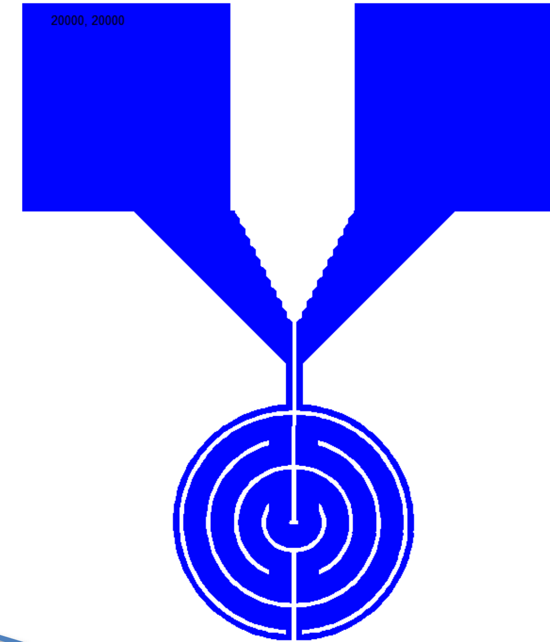


4 μm PECVD SiO_2 Deposition

Process Flow

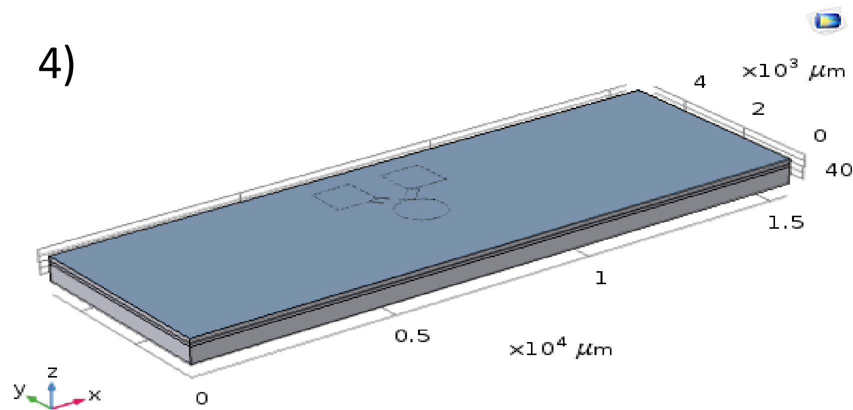
3)





Heater : Lithography + TI/PT Deposition &Lift-Off

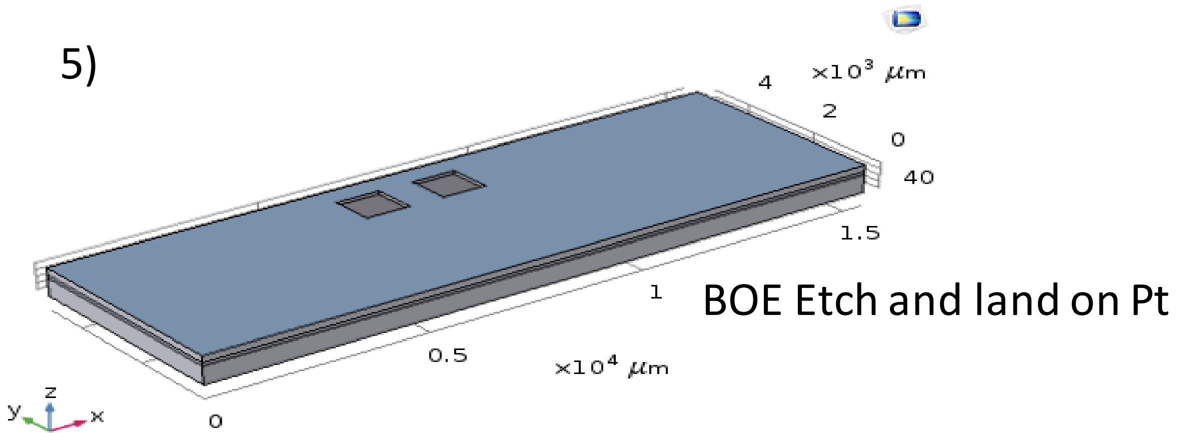
4)



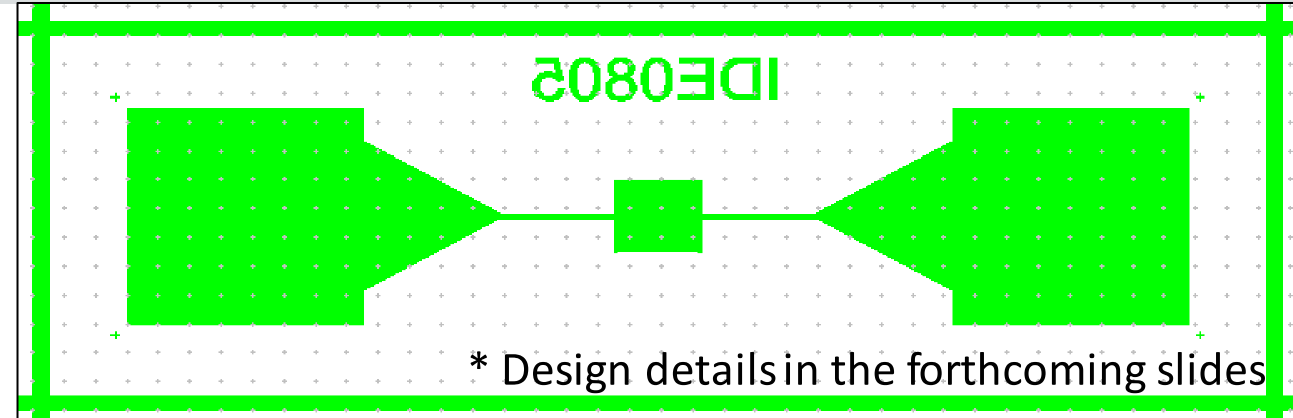
500nm PECVD Oxide Deposition

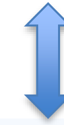
Process Flow

5)



BOE Etch and land on Pt





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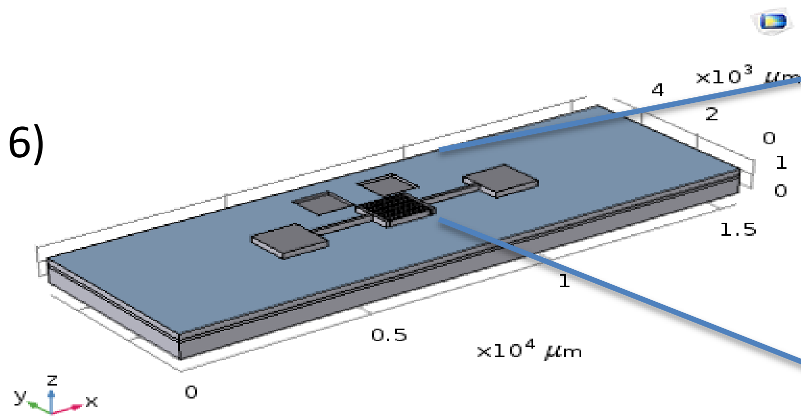
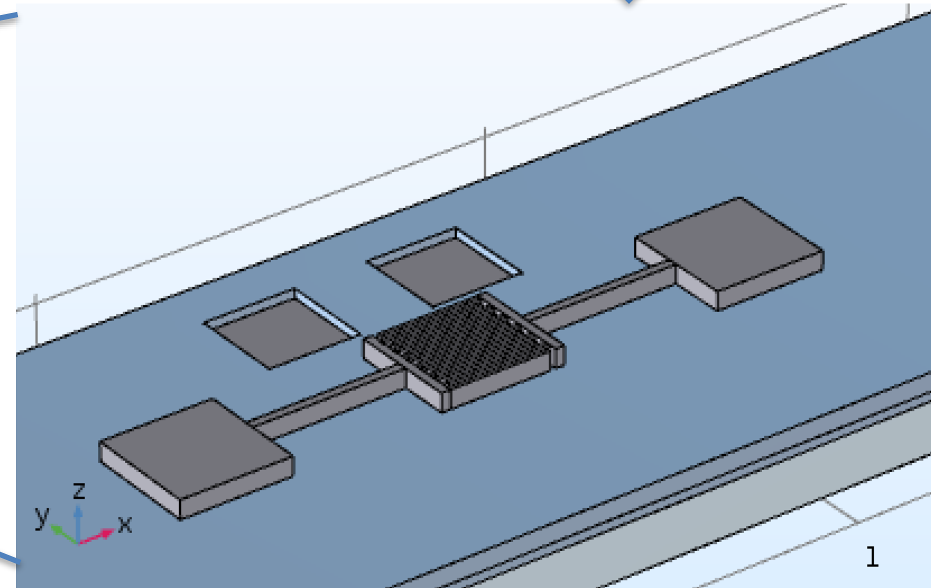


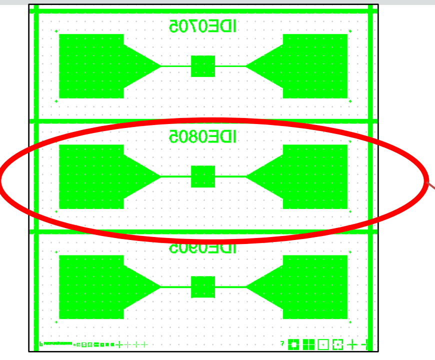


IDE : Lithography +
TI/PT Deposition &Lift-Off

IDE details for measurement

Design Specification	Comments
IDE	5um
Gap between IDE	5um
IDE electrode Length	1020um
No of fingers in IDE	100
Electrode pads	3mmX3mm
IDE to Pad distance	3.2mm
IDE-Pad connecting line width	60um (near IDE) increasing to 2.07mm(near electrode pad)
Contact pad lead out pattern	Linear
Device Size	3mmX13.5mm

Single Die details



IDE0805

1.1 mm

3mm

1mm

3mm

3mm

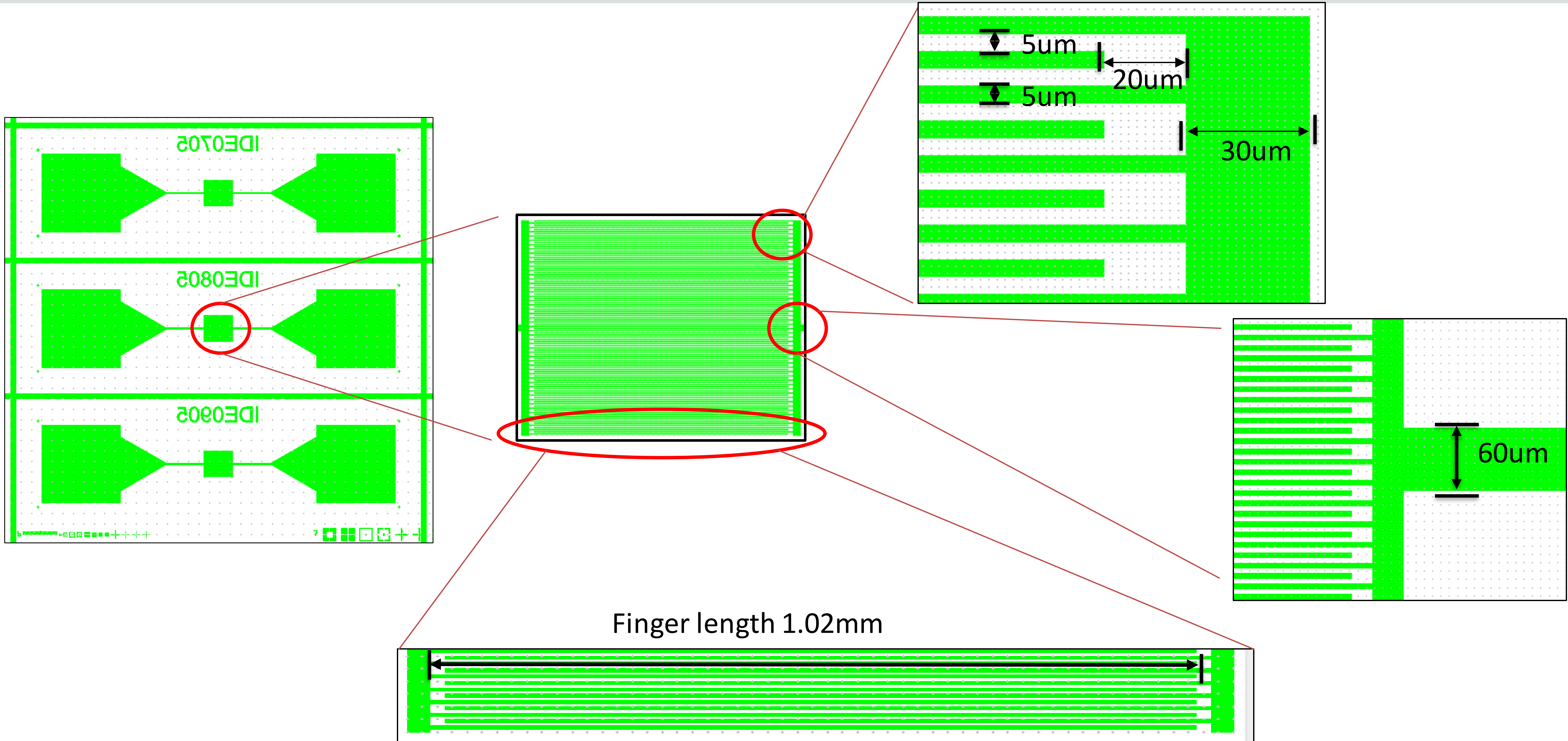
3.2mm

3.2mm

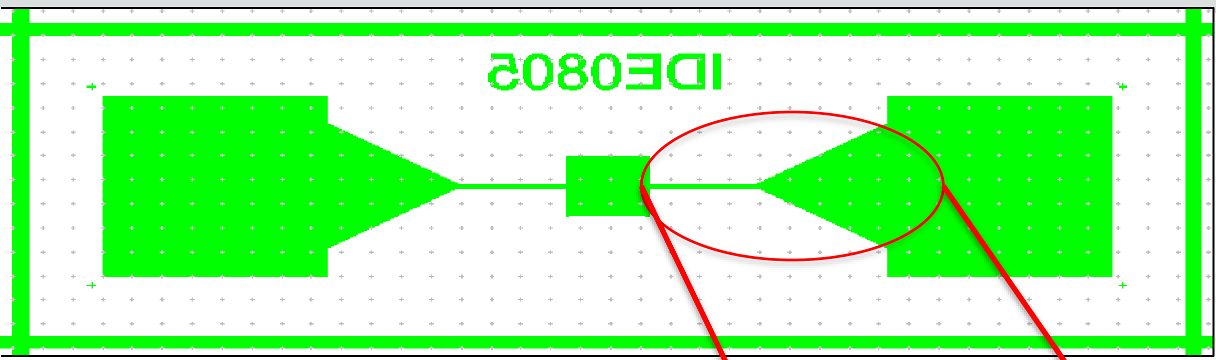
3mm

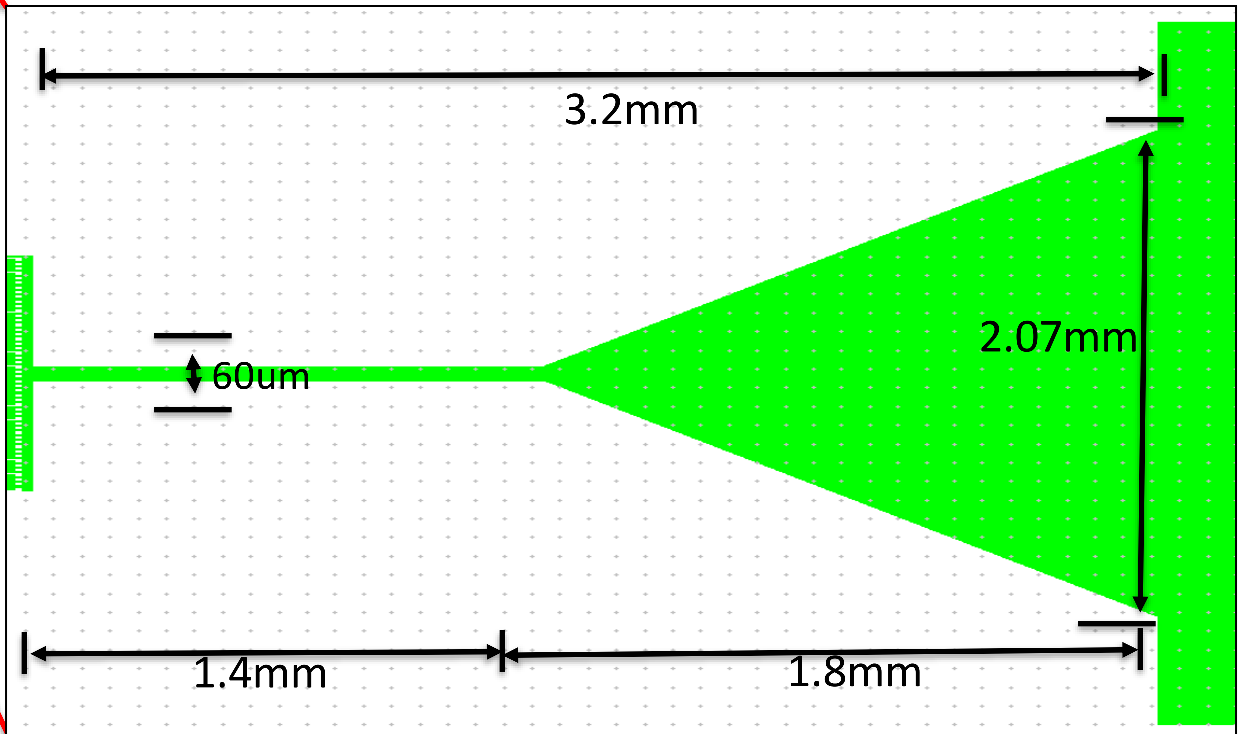
200um

IDE Details

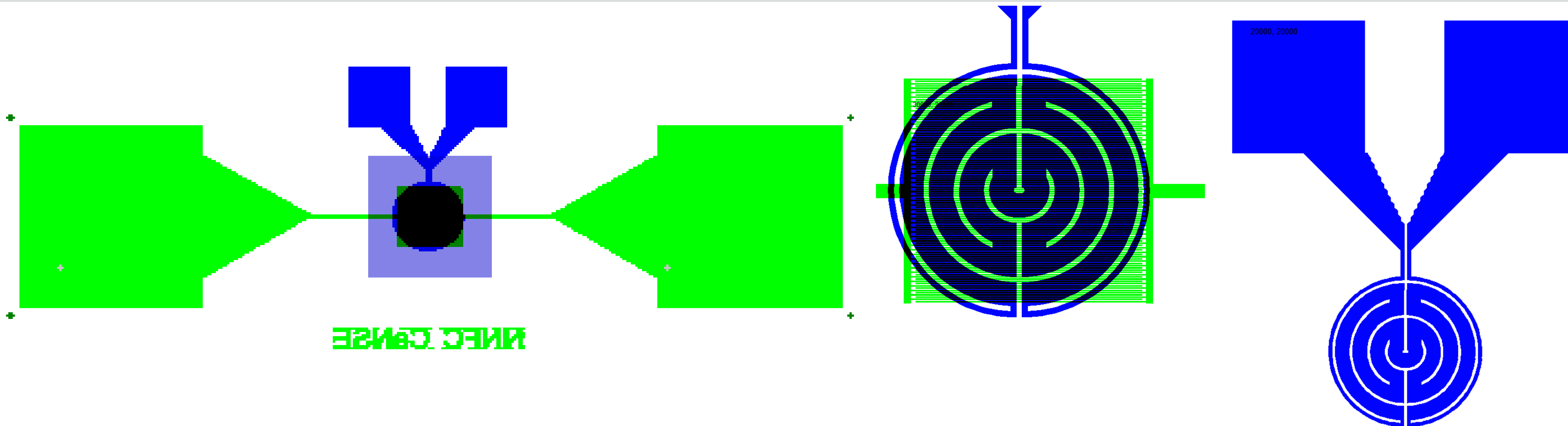


IDE to Electrode Pad Connector Details





IDE with Heater



Thank You

PI Team