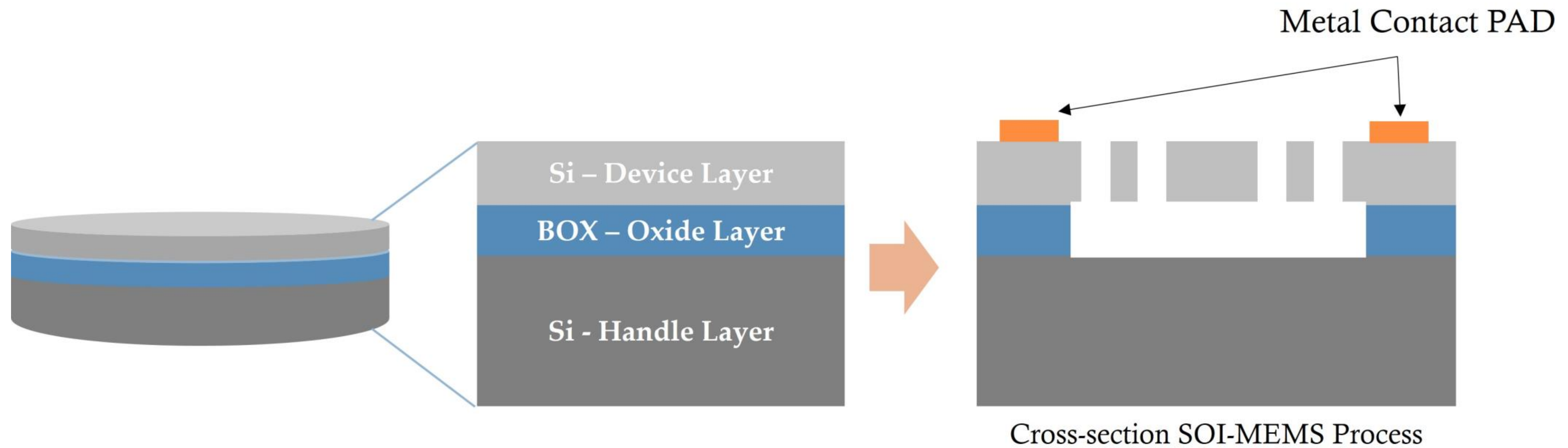
SOI-MEMS Foundry Services at CeNSE

One step solution for MEMS Manufacturing

MPW | CeNSE | Sudhanshu Shekhar

SOI-MEMS Process

- **Silicon-On-Insulator (SOI) Wafer**

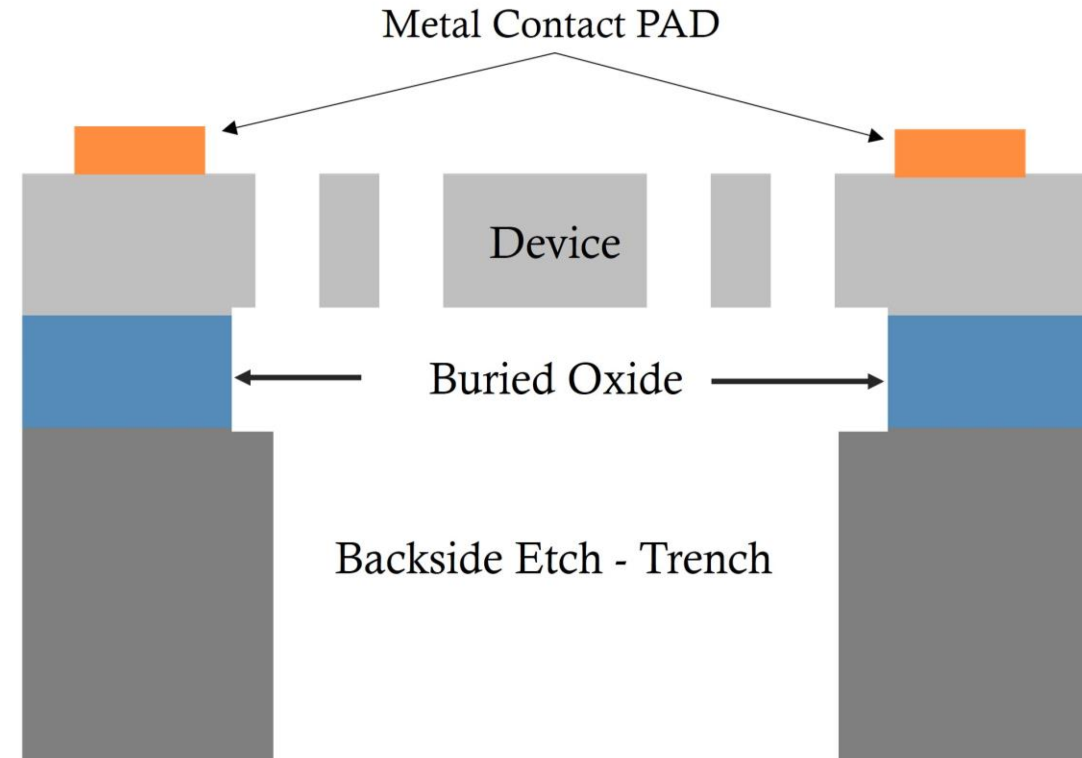


Cross-section SOI-MEMS Process

SOI-MEMS Process

- **Layer features:**

Metal PAD layer : 0.2 - 0.4 μm
Device layer : 20 μm
Buried Oxide : 1 - 2 μm
Handle layer : 500 μm



Cross-section SOI-MEMS Process

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SOI-MEMS Process

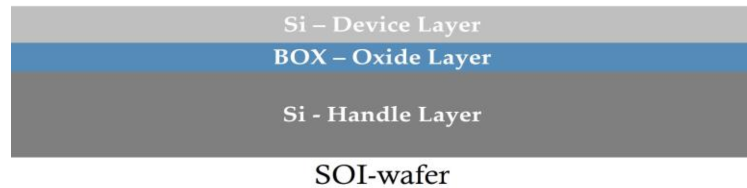
- **Layer feature:**

  - Device layer thickness (SOI): 20 μm
  - Handle layer thickness (Si): 500 μm
  - Buried oxide (BOX): 1 – 2 μm

- Device layer is used to fabricate mechanical structures such as – cantilever, resonators, resistors
- Buried oxide (BOX) acts as a sacrificial layer which is removed using HF to release the structure
- Contact PAD Au/Cr (20/200 nm) deposited on top of device layer to make electrical connections
- Handle layer or substrate is used to provide mechanical strength

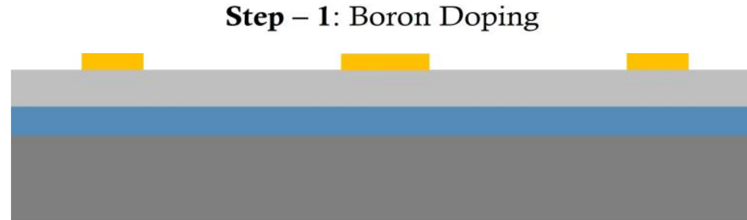
SOI-MEMS Process

- **Process Flow:**

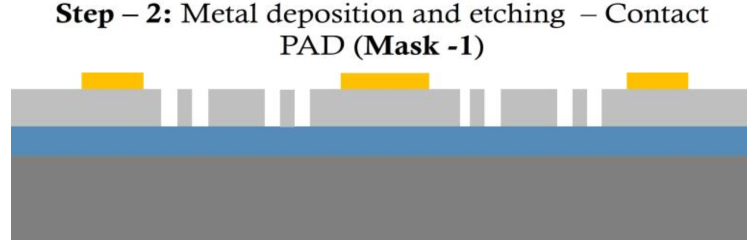


SOI-wafer

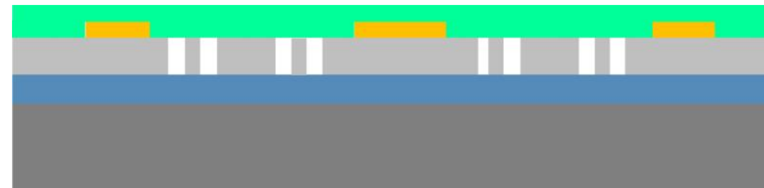
Step – 1: Boron Doping



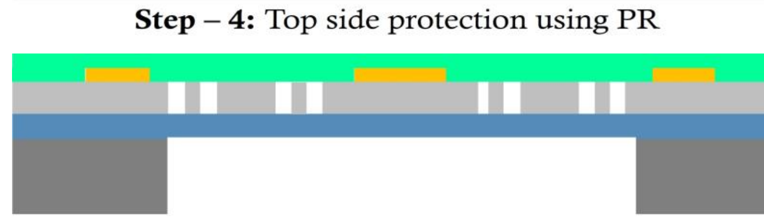
Step – 2: Metal deposition and etching – Contact PAD (**Mask -1**)



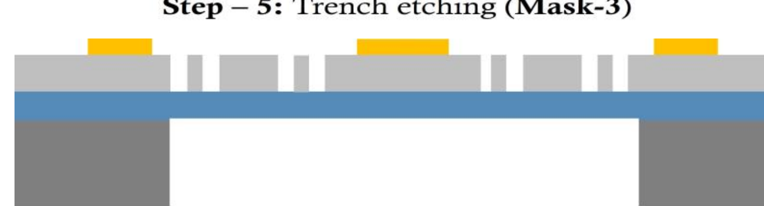
Step – 3: Structural layer etching DRIE (**Mask -2**)



Step – 4: Top side protection using PR



Step – 5: Trench etching (**Mask-3**)



Step – 6: PR Strip

Step – 7: BOX removal using HF

Photo-resist
Metal
Oxide
Silicon
Silicon

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Design Rules (1)

- SOI-MEMS is a 3-mask process.
- Device layer is of single-crystal-silicon (SCS) with a thickness of 20 μm.
- The resistivity of device layer is in the range of 1 – 30 Ohm – cm (Ω-cm).

Layer	Material	Thickness	Remark
L0 – Metal PAD	Cr/Au	20/200 nm	Electrical contact - Bond-pad
L1 – SOI	Si	20 μm ± 0.5 μm	Mechanical structures - Beams, Resonators etc.
L2 – BOX	Oxide	1 – 2 μm ± 0.1 μm	Sacrificial layer
L3 – Handle wafer	Si	500 μm ± 10 μm	Mechanical support

Design Rules (2)

- Key points to remember before staring any design -
- **Critical dimension (CD)** and Mnemonics associated with each layer

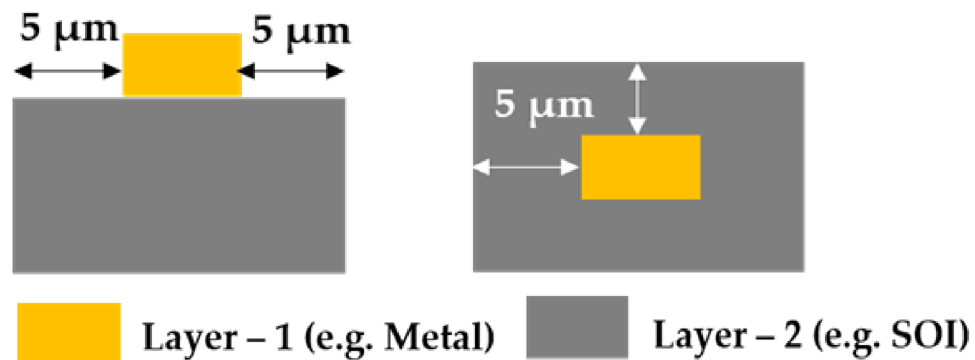
Mnemonics	Layer Name	Min. Feature (μm)	Min. Space (μm)
MetalPAD	CPAD	5	5
SOI	SOI	3	5
SOIHOLE	HOLE	10	5
TRENCH	TRNCH	200	100

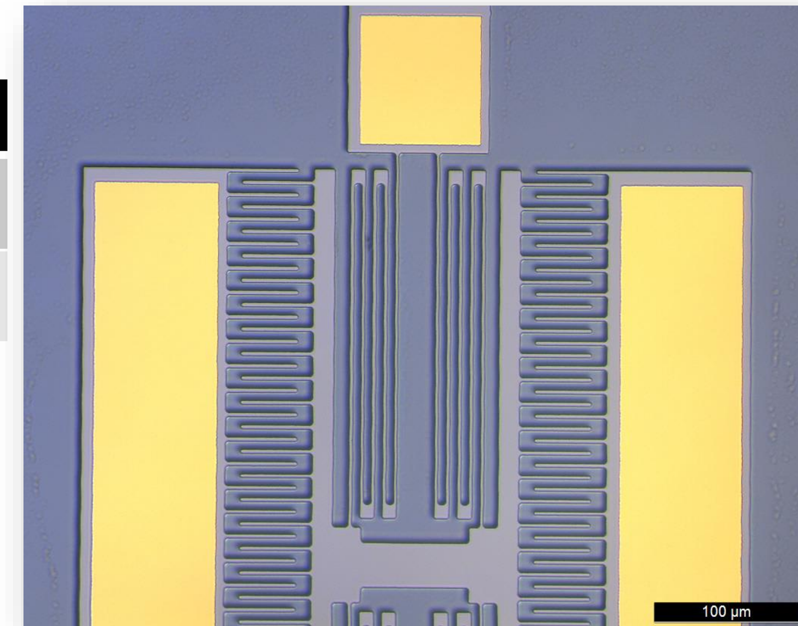
Design Rules (3)

- Key points to remember before staring any design -

- Overlay between two layers

Layer	Center-to-Center (µm)	Edge-to-Edge (µm)
MetalPAD to SOI	± 5	± 5
TRENCH to SOI	± 5	± 50





Metal contact PAD (yellow in color) on top of device layer for electrical contact

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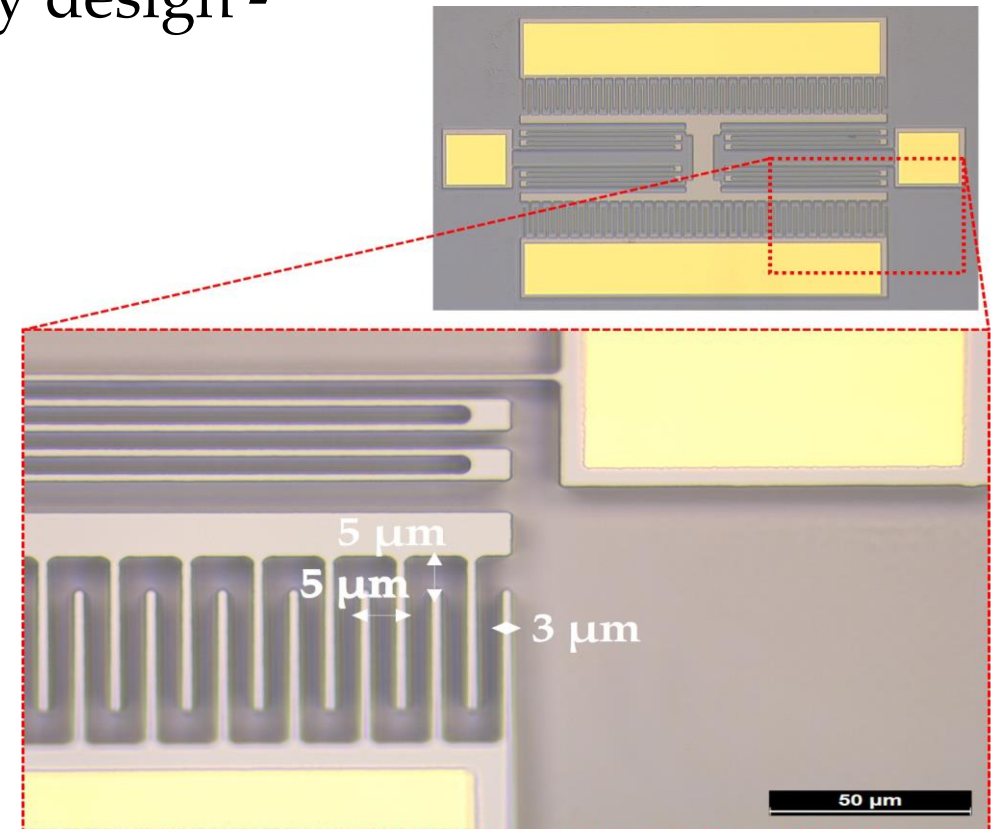
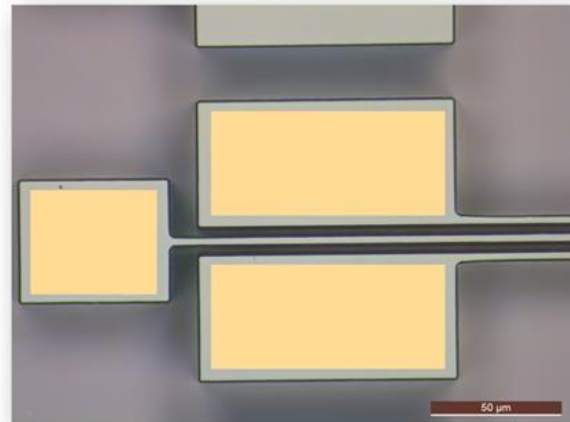
Design Rules (4)

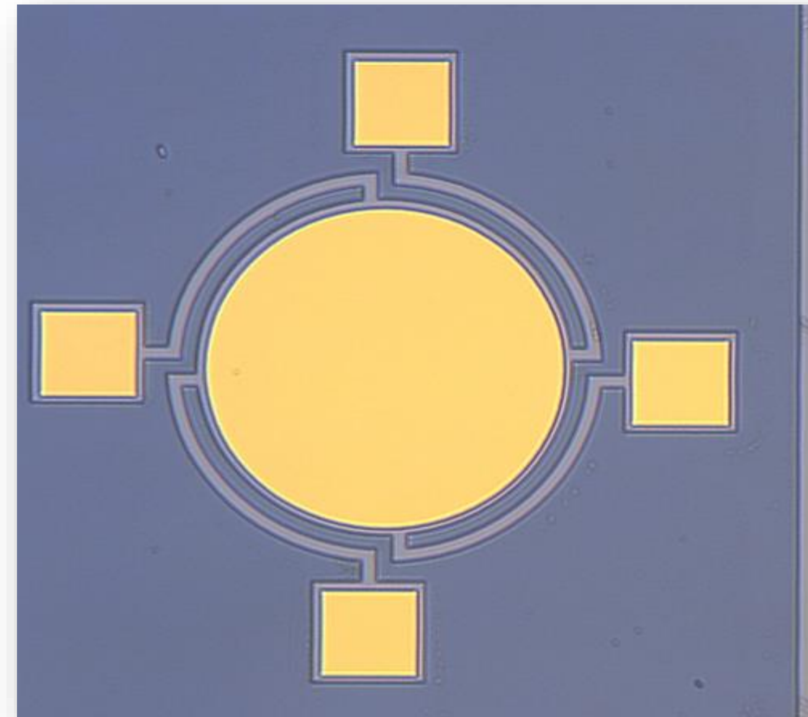
- Key points to remember before staring any design -
- Recommended design format – CIF or GDS
- **Critical Dimension (CD)**
  - **Min. feature size of microstructures – 3 μm**
- Minimum spacing between two adjacent microstructures (gap between two comb fingers in case of an electrostatic comb-drive actuator) **should not be less than 5 μm** (see adjacent figures for reference)



Design Rules (5)

- Key points to remember before staring any design -
- Contact **PAD** recommended dimension (see figures for reference)
  - **On-wafer probe – 200 μm × 200 μm**
  - **Bond-pad – 500 μm × 500 μm (wire-bonding)**

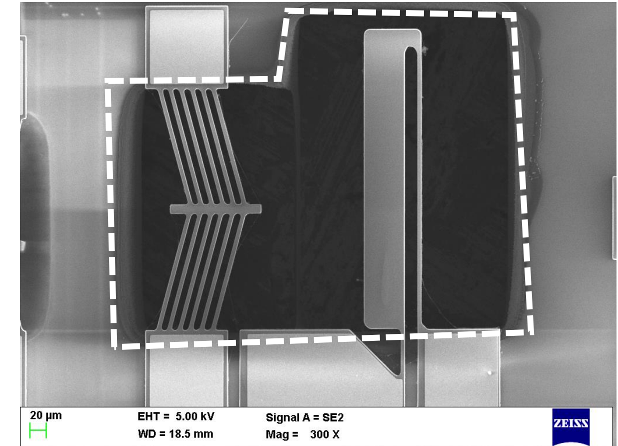


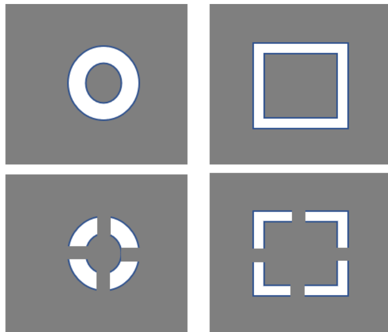


Metal contact PAD (yellow) on top of device layer for electrical contact

Design Rules (6)

- Key points to remember before staring any design -
- **TRENCH -**
  - No un-anchored structure under the TRENCH
  - Minimum feature size – **100 µm × 100 µm**
  - Center-to-Center – **≤ 50 µm** (Top-to-Bottom Alignment)





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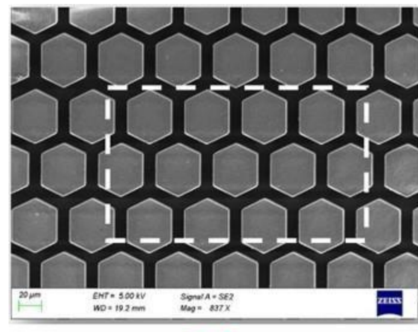

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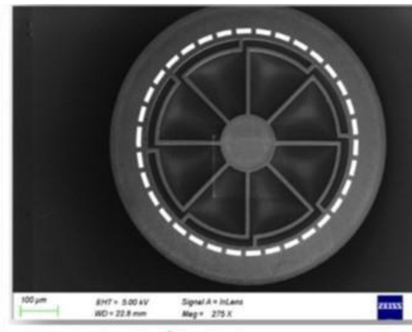

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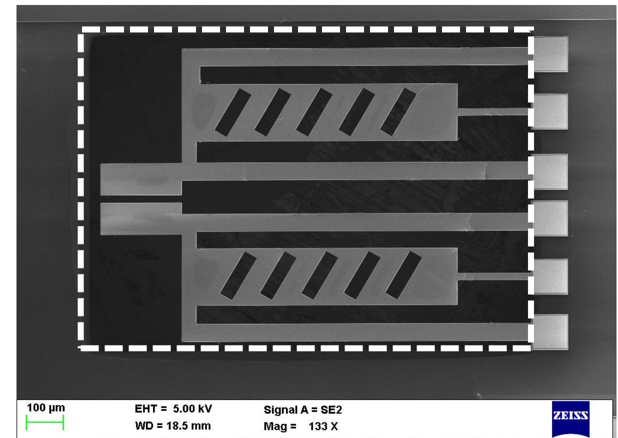


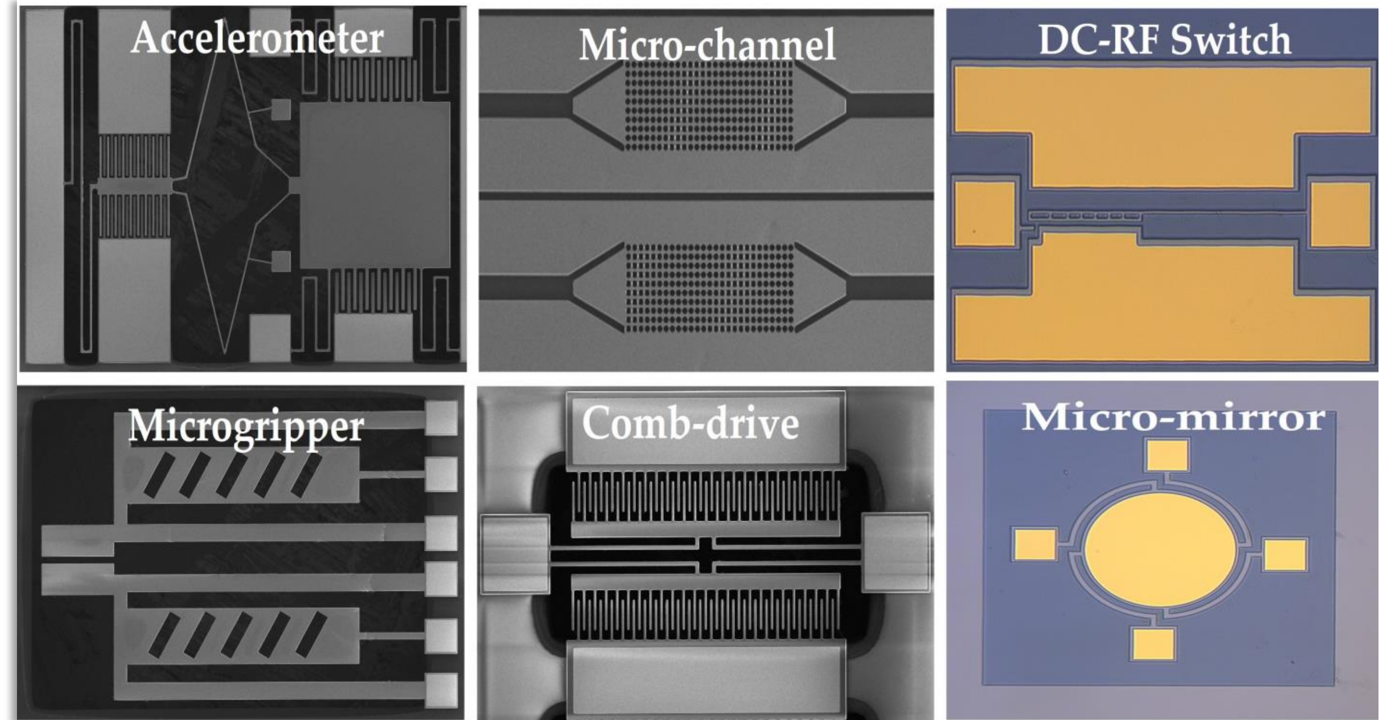
Design Rules (7)

- Design layout can be created using any layout editor such as L-edit, K-layout, Clewin, Mentor Graphics and others
- Accepted design formats are CIF and GDS-II
- Users must convert their final designs for the fabrication should be either CIF or GDS-II

What all you can fabricate?

MEMS devices :-

- Inertial Sensors –
  - Gyroscope
  - Accelerometer
- DC-RF Switches
- Thermal Actuator
- Resonator, Oscillator
- Optical Switches, Waveguides
- Microfluidic Channels



Some of the MEMS devices fabricated using SOI-MEMS Process